



VND7N04/VND7N04-1 VNP7N04FI/K7N04FM

"OMNIFET": FULLY AUTOPROTECTED POWER MOSFET

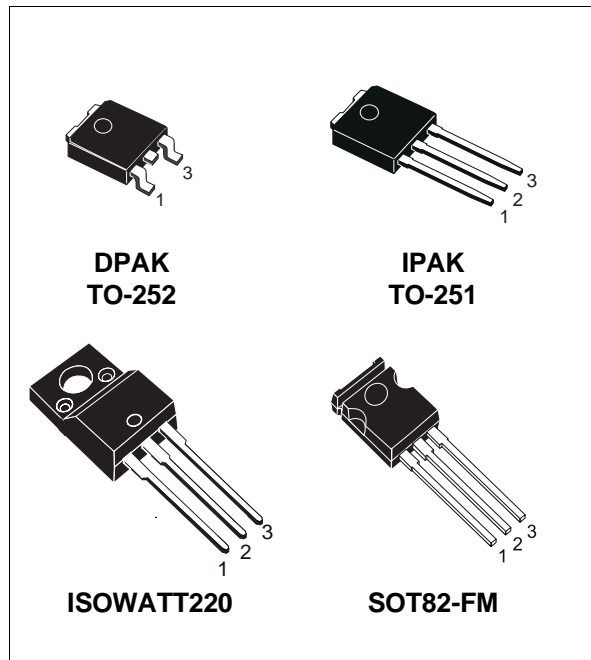
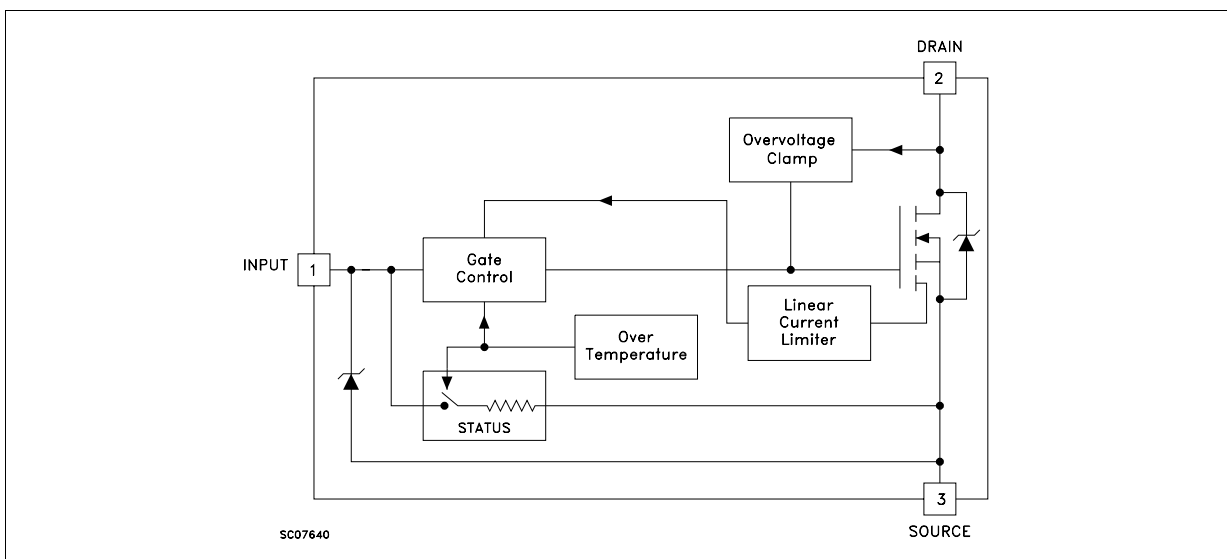
TYPE	V _{clamp}	R _{DS(on)}	I _{lim}
VND7N04	42 V	0.14 Ω	7 A
VND7N04-1	42 V	0.14 Ω	7 A
VNP7N04FI	42 V	0.14 Ω	7 A
VNK7N04FM	42 V	0.14 Ω	7 A

- LINEAR CURRENT LIMITATION
- THERMAL SHUT DOWN
- SHORT CIRCUIT PROTECTION
- INTEGRATED CLAMP
- LOW CURRENT DRAWN FROM INPUT PIN
- DIAGNOSTIC FEEDBACK THROUGH INPUT PIN
- ESD PROTECTION
- DIRECT ACCESS TO THE GATE OF THE POWER MOSFET (ANALOG DRIVING)
- COMPATIBLE WITH STANDARD POWER MOSFET

DESCRIPTION

The VND7N04, VND7N04-1, VNP7N04FI and VNK7N04FM are monolithic devices made using STMicroelectronics VIPower M0 Technology, intended for replacement of standard power MOSFETS in DC to 50 KHz applications. Built-in thermal shut-down, linear current limitation and overvoltage clamp protect the chip in harsh

BLOCK DIAGRAM



environments.

Fault feedback can be detected by monitoring the voltage at the input pin.

VND7N04/VND7N04-1/VNP7N04FI/VNK7N04FM

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value			Unit
		DPAK IPAK	ISOWATT220	SOT-82FM	
V _{DS}	Drain-source Voltage (V _{in} = 0)	Internally Clamped			V
V _{in}	Input Voltage	18			V
I _D	Drain Current	Internally Limited			A
I _R	Reverse DC Output Current	-7			A
V _{esd}	Electrostatic Discharge (C= 100 pF, R=1.5 KΩ)	2000			V
P _{tot}	Total Dissipation at T _c = 25 °C	60	24	9	W
T _j	Operating Junction Temperature	Internally Limited			°C
T _c	Case Operating Temperature	Internally Limited			°C
T _{stg}	Storage Temperature	-55 to 150			°C

THERMAL DATA

		DPAK/IPAK	ISOWATT220	SOT82-FM	
R _{thj-case}	Thermal Resistance Junction-case Max	3.75	5.2	14	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient Max	100	62.5	100	°C/W

ELECTRICAL CHARACTERISTICS (-40 < T_j < 125 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{CLAMP}	Drain-source Clamp Voltage	I _D = 200 mA V _{in} = 0	32	42	52	V
V _{CLTH}	Drain-source Clamp Threshold Voltage	I _D = 2 mA V _{in} = 0	31			V
V _{INCL}	Input-Source Reverse Clamp Voltage	I _{in} = -1 mA	-1.1		-0.25	V
I _{DSS}	Zero Input Voltage Drain Current (V _{in} = 0)	V _{DS} = 13 V V _{in} = 0 V _{DS} = 25 V V _{in} = 0			75 200	μA μA
I _{ISS}	Supply Current from Input Pin	V _{DS} = 0 V V _{in} = 10 V		250	550	μA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{IN(th)}	Input Threshold Voltage	V _{DS} = V _{in} I _D + I _{in} = 1 mA	0.8		3	V
R _{DS(on)}	Static Drain-source On Resistance	V _{in} = 10 V I _D = 3.5 A V _{in} = 5 V I _D = 3.5 A -40 < T _j < 25 °C V _{in} = 10 V I _D = 3.5 A V _{in} = 5 V I _D = 3.5 A T _j = 125 °C			0.14 0.28 0.28 0.56	Ω Ω Ω Ω

ELECTRICAL CHARACTERISTICS (continued)

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (*)	Forward Transconductance	$V_{DS} = 13\text{ V}$ $I_D = 3.5\text{ A}$	2	5		S
C_{oss}	Output Capacitance	$V_{DS} = 13\text{ V}$ $f = 1\text{ MHz}$ $V_{in} = 0$		250	500	pF

SWITCHING ()**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 15\text{ V}$ $I_d = 3.5\text{ A}$ $V_{gen} = 10\text{ V}$ $R_{gen} = 10\ \Omega$		50 60	150 180	ns ns
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	(see figure 3)		130 50	300 200	ns ns
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 15\text{ V}$ $I_d = 3.5\text{ A}$ $V_{gen} = 10\text{ V}$ $R_{gen} = 1000\ \Omega$		140 0.4	500 1.1	ns μs
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	(see figure 3)		2.5 1	7 4	μs μs
$(di/dt)_{on}$	Turn-on Current Slope	$V_{DD} = 15\text{ V}$ $I_D = 3.5\text{ A}$ $V_{in} = 10\text{ V}$ $R_{gen} = 10\ \Omega$		50		A/ μs
Q_i	Total Input Charge	$V_{DD} = 12\text{ V}$ $I_D = 3.5\text{ A}$ $V_{in} = 10\text{ V}$		18		nC

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{SD} (*)	Forward On Voltage	$I_{SD} = 3.5\text{ A}$ $V_{in} = 0$			1.7	V
t_{rr} (**)	Reverse Recovery Time	$I_{SD} = 3.5\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 30\text{ V}$ $T_j = 25\text{ }^\circ\text{C}$		40		ns
Q_{rr} (**)	Reverse Recovery Charge	(see test circuit, figure 5)		0.2		μC
I_{RRM} (**)	Reverse Recovery Current			3.6		A

PROTECTION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{lim}	Drain Current Limit	$V_{in} = 10\text{ V}$ $V_{DS} = 13\text{ V}$ $V_{in} = 5\text{ V}$ $V_{DS} = 13\text{ V}$	4 4	7 7	11 11	A A
t_{dlim} (**)	Step Response Current Limit	$V_{in} = 10\text{ V}$ $V_{in} = 5\text{ V}$		13 15	20 25	μs μs
T_{jsh} (**)	Overtemperature Shutdown		150			$^\circ\text{C}$
T_{jrs} (**)	Overtemperature Reset		135			$^\circ\text{C}$
I_{gf} (**)	Fault Sink Current	$V_{in} = 10\text{ V}$ $V_{DS} = 13\text{ V}$ $V_{in} = 5\text{ V}$ $V_{DS} = 13\text{ V}$		50 20		mA mA
E_{as} (**)	Single Pulse Avalanche Energy	starting $T_j = 25\text{ }^\circ\text{C}$ $V_{DD} = 20\text{ V}$ $V_{in} = 10\text{ V}$ $R_{gen} = 1\text{ K}\Omega$ $L = 30\text{ mH}$	0.4			J

(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

(**) Parameters guaranteed by design/characterization

PROTECTION FEATURES

During normal operation, the Input pin is electrically connected to the gate of the internal power MOSFET. The device then behaves like a standard power MOSFET and can be used as a switch from DC to 50 KHz. The only difference from the user's standpoint is that a small DC current (I_{ISS}) flows into the Input pin in order to supply the internal circuitry.

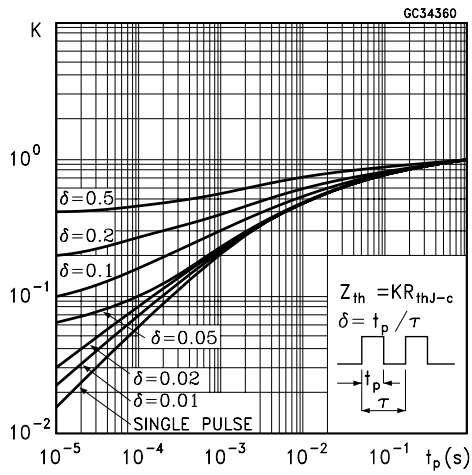
The device integrates:

- **OVERVOLTAGE CLAMP PROTECTION:** internally set at 42V, along with the rugged avalanche characteristics of the Power MOSFET stage give this device unrivalled ruggedness and energy handling capability. This feature is mainly important when driving inductive loads.
- **LINEAR CURRENT LIMITER CIRCUIT:** limits the drain current I_d to I_{lim} whatever the Input pin voltage. When the current limiter is active, the device operates in the linear region, so power dissipation may exceed the capability of the heatsink. Both case and junction temperatures increase, and if this phase lasts long enough, junction temperature may reach the overtemperature threshold T_{jsh} .

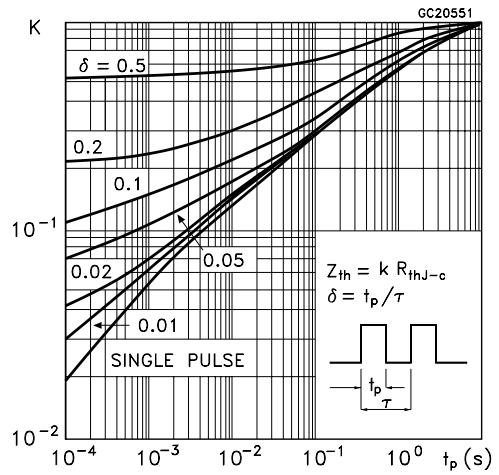
- **OVERTEMPERATURE AND SHORT CIRCUIT PROTECTION:** these are based on sensing the chip temperature and are not dependent on the input voltage. The location of the sensing element on the chip in the power stage area ensures fast, accurate detection of the junction temperature. Overtemperature cutout occurs at minimum 150°C. The device is automatically restarted when the chip temperature falls below 135°C.
- **STATUS FEEDBACK:** In the case of an overtemperature fault condition, a Status Feedback is provided through the Input pin. The internal protection circuit disconnects the input from the gate and connects it instead to ground via an equivalent resistance of 100 Ω . The failure can be detected by monitoring the voltage at the Input pin, which will be close to ground potential.

Additional features of this device are ESD protection according to the Human Body model and the ability to be driven from a TTL Logic circuit (with a small increase in $R_{DS(on)}$).

Thermal Impedance For DPAK / IPAK



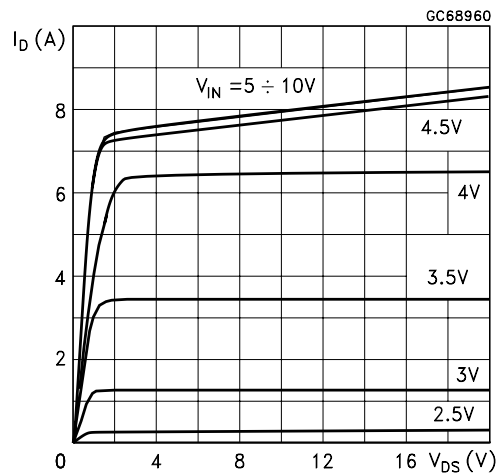
Thermal Impedance For ISOWATT220



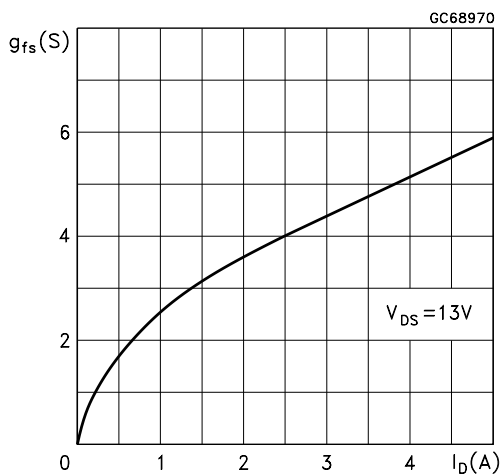
Derating Curve



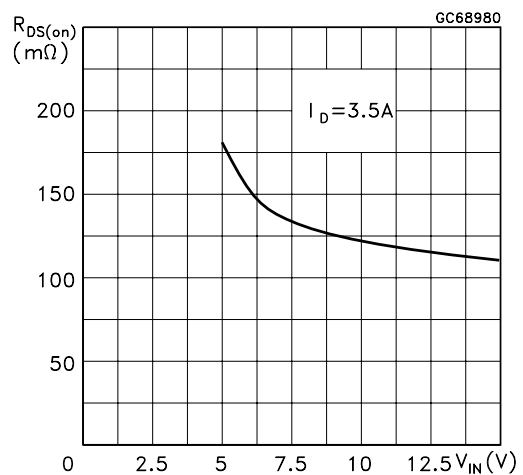
Output Characteristics



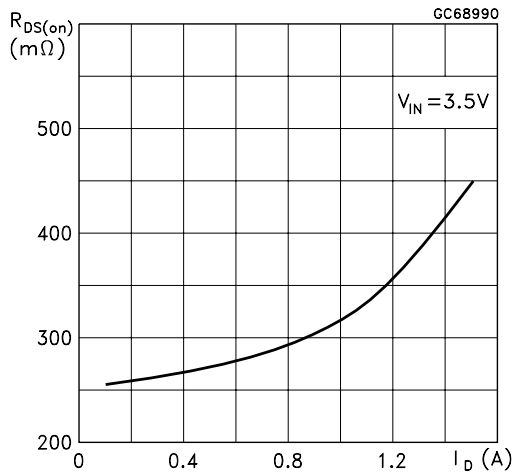
Transconductance



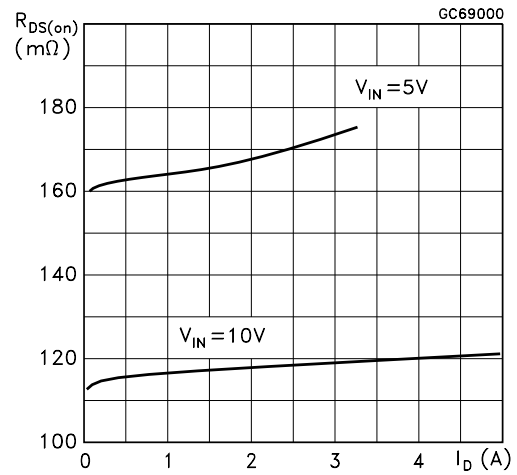
Static Drain-Source On Resistance vs Input Voltage



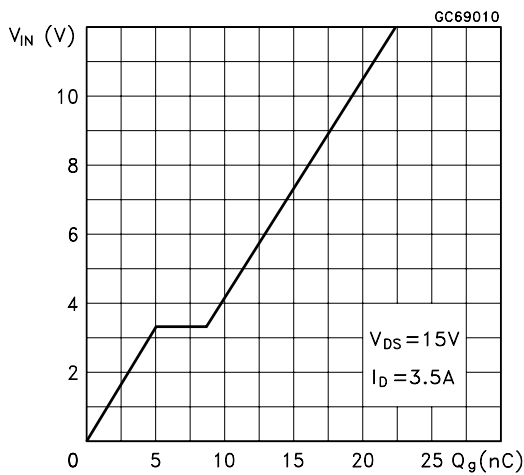
Static Drain-Source On Resistance



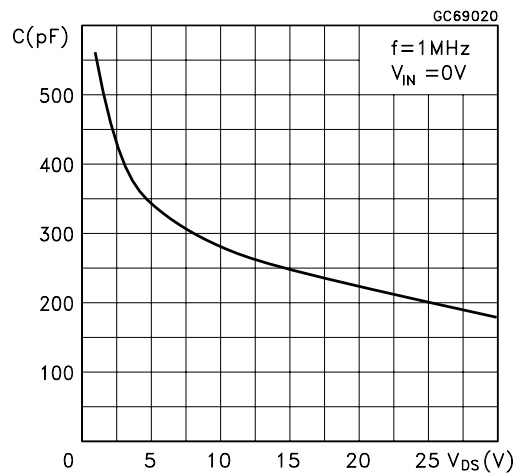
Static Drain-Source On Resistance



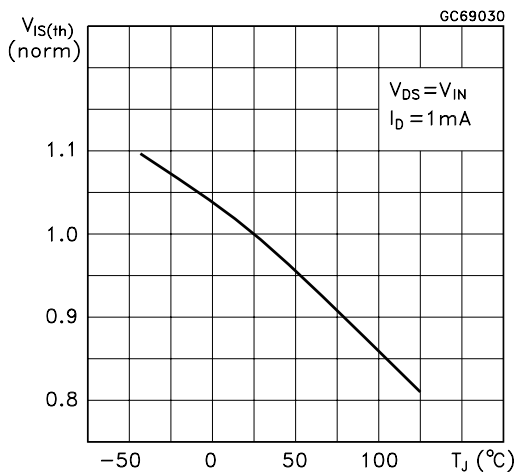
Input Charge vs Input Voltage



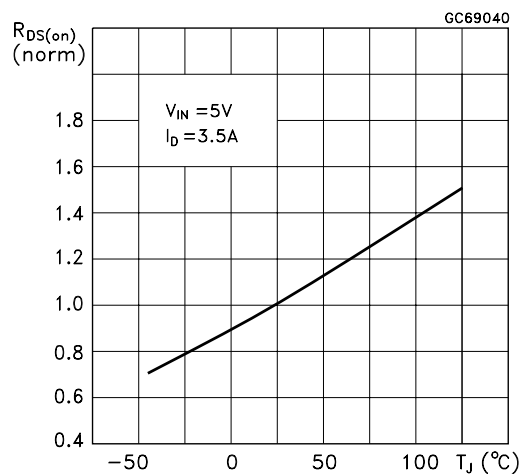
Capacitance Variations



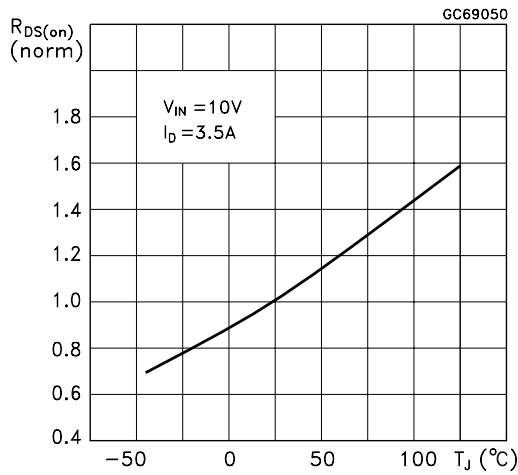
Normalized Input Threshold Voltage vs Temperature



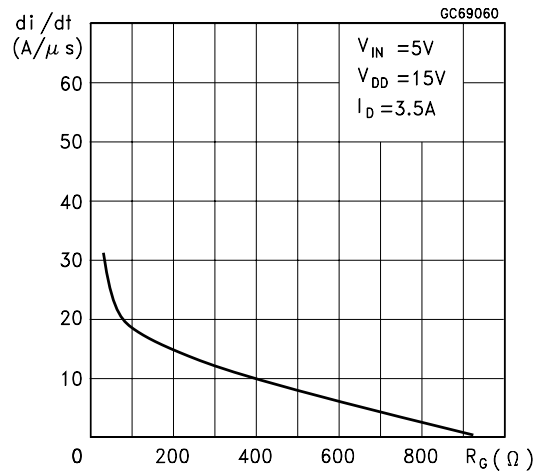
Normalized On Resistance vs Temperature



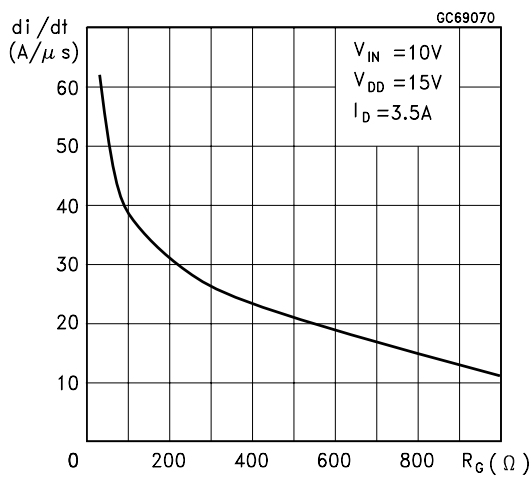
Normalized On Resistance vs Temperature



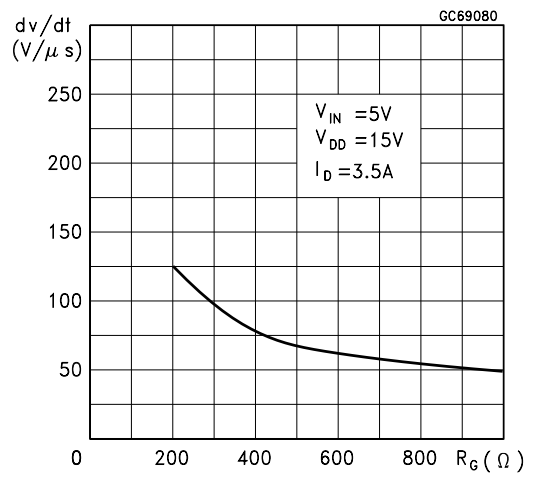
Turn-on Current Slope



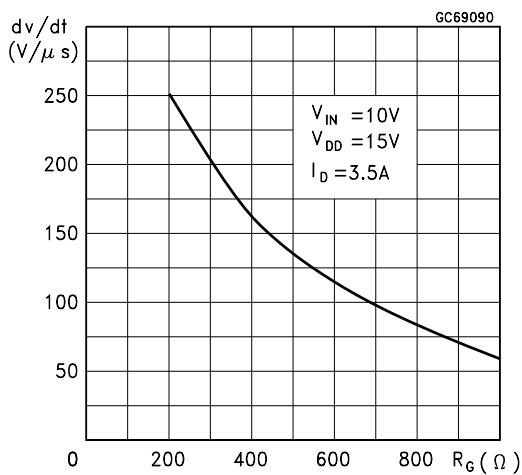
Turn-on Current Slope



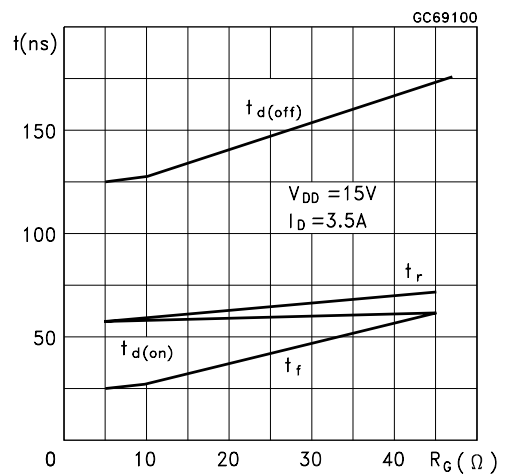
Turn-off Drain-Source Voltage Slope



Turn-off Drain-Source Voltage Slope

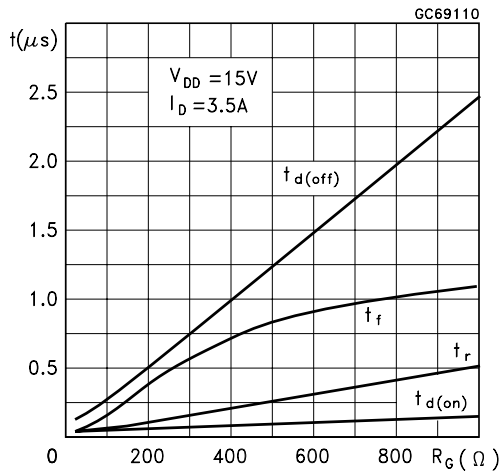


Switching Time Resistive Load

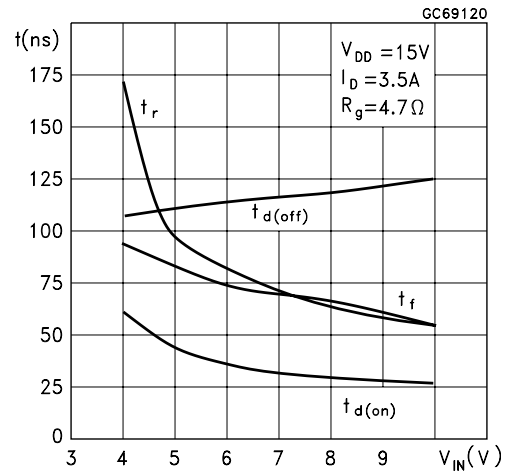


VND7N04/VND7N04-1/VNP7N04FI/VNK7N04FM

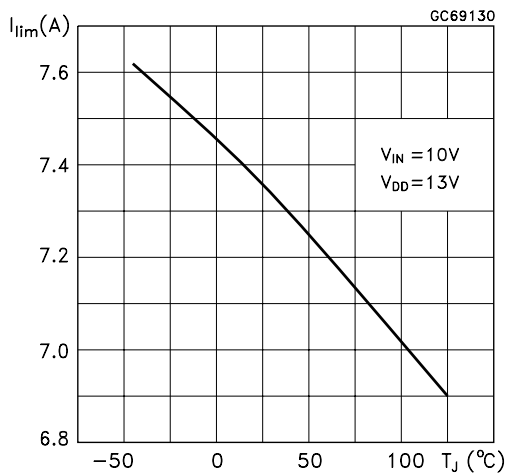
Switching Time Resistive Load



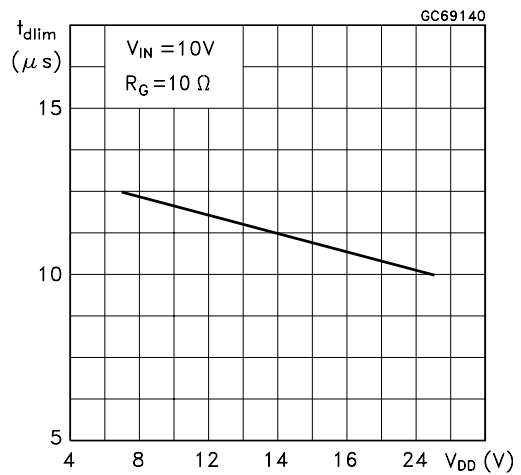
Switching Time Resistive Load



Current Limit vs Junction Temperature



Step Response Current Limit



Source Drain Diode Forward Characteristics

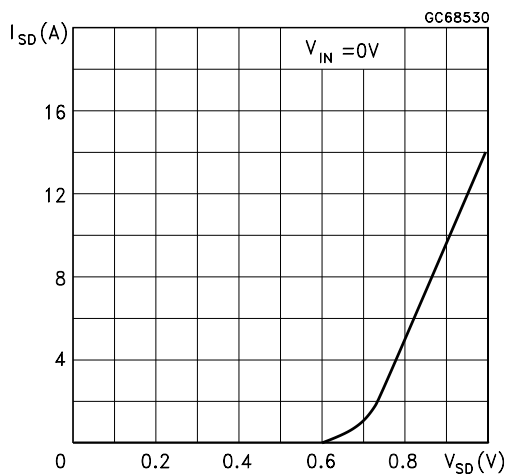


Fig. 1: Unclamped Inductive Load Test Circuits



Fig. 2: Unclamped Inductive Waveforms

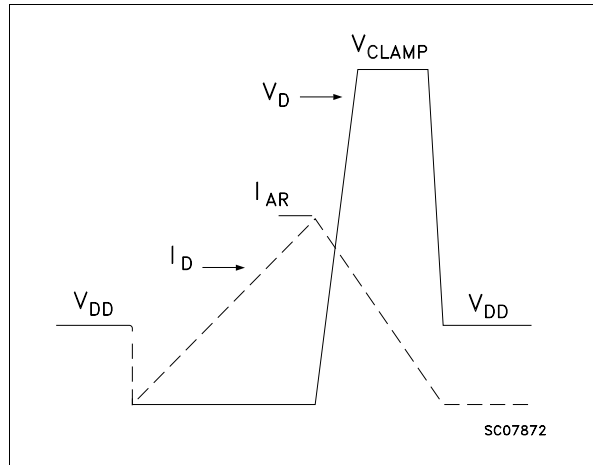


Fig. 3: Switching Times Test Circuits For Resistive Load



Fig. 4: Input Charge Test Circuit

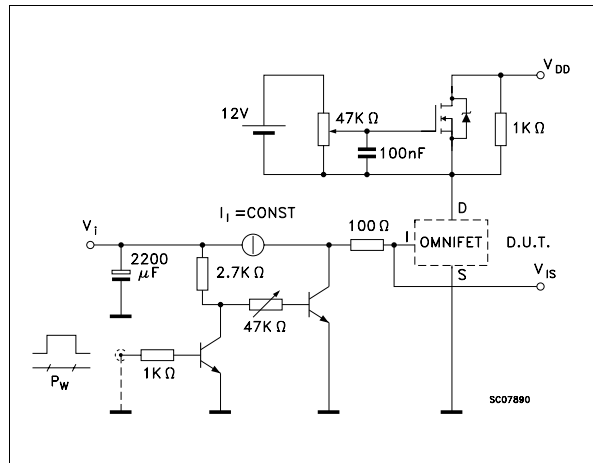


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times

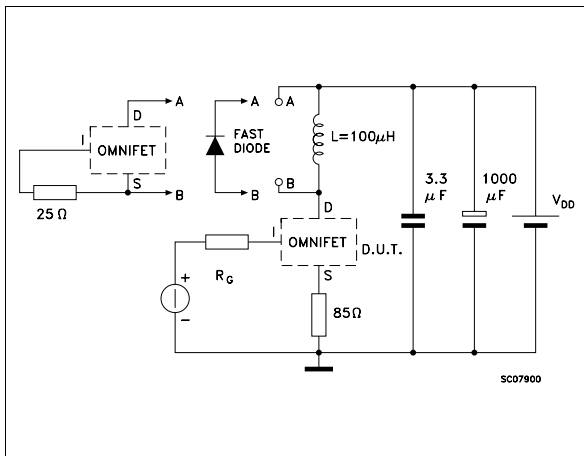
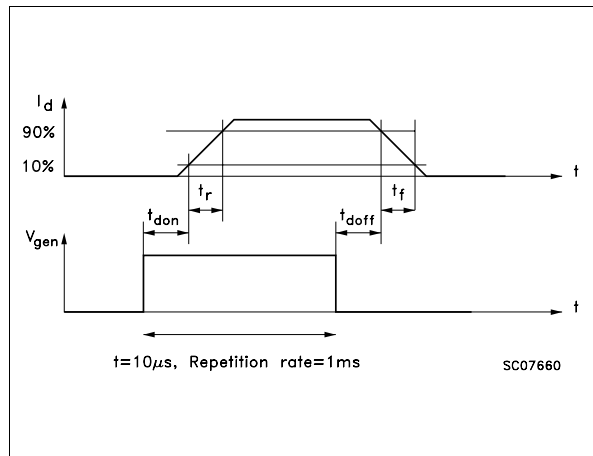
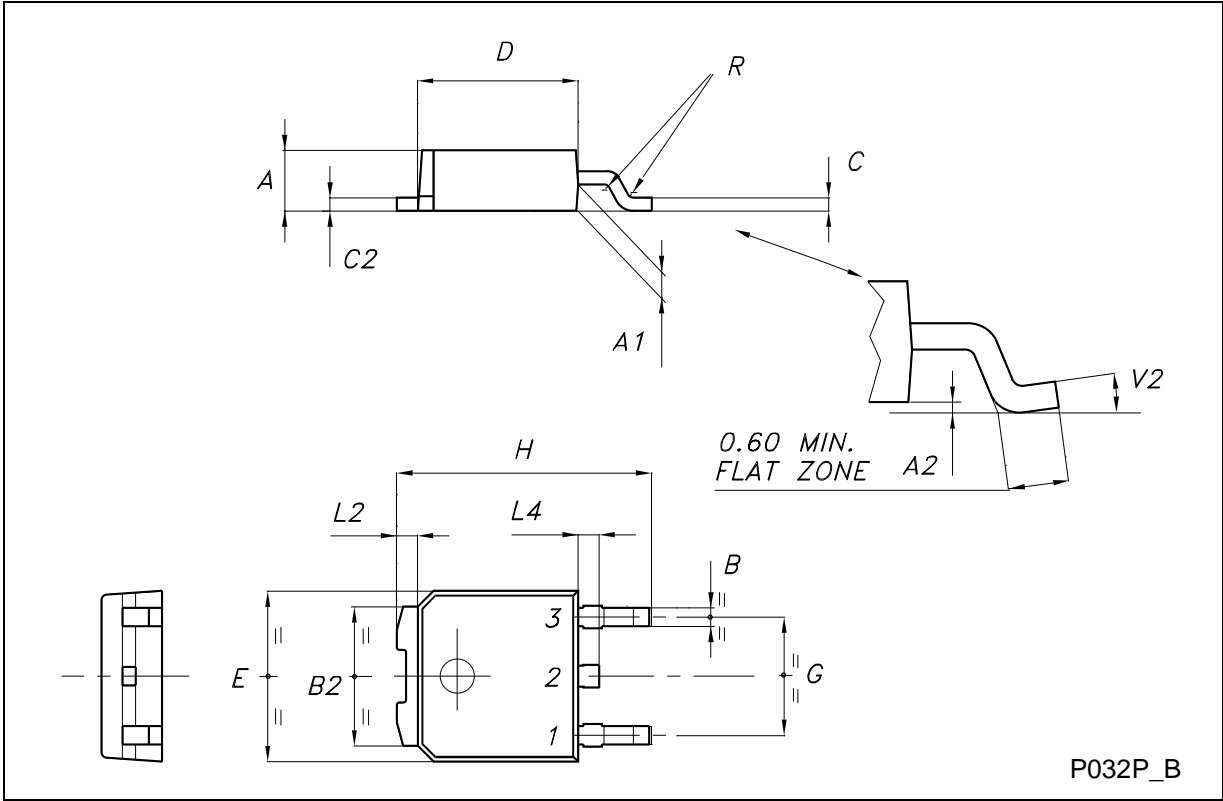


Fig. 6: Waveforms



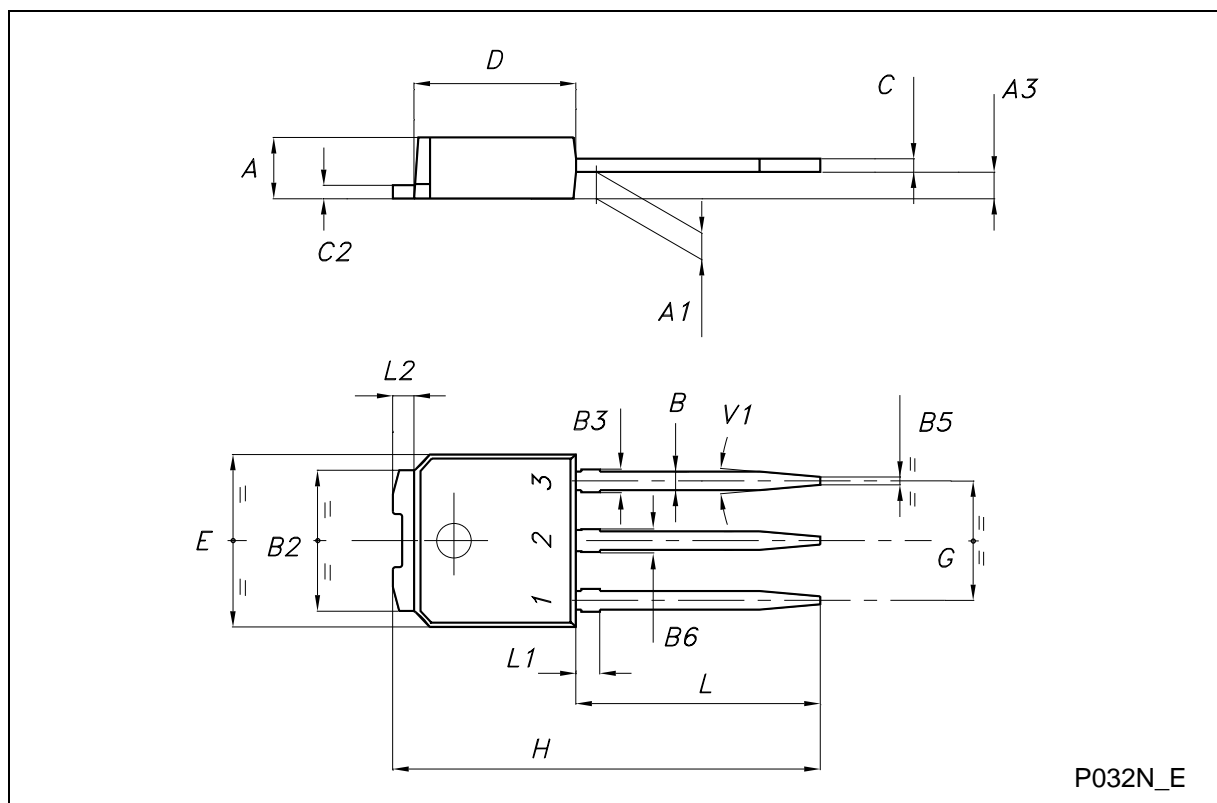
TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
C	0.45		0.60	0.018		0.024
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	9.35		10.10	0.368		0.398
L2		0.8			0.031	
L4	0.60		1.00	0.024		0.039
V2	0°		8°	0°		0°



TO-251 (IPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A3	0.70		1.30	0.028		0.051
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
B3			0.85			0.033
B5		0.30			0.012	
B6			0.95			0.037
C	0.45		0.60	0.018		0.024
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.237		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	15.90		16.30	0.626		0.642
L	9.00		9.40	0.354		0.370
L1	0.80		1.20	0.031		0.047
L2		0.80	1.00		0.031	0.039
V1		10°			10°	



P032N_E

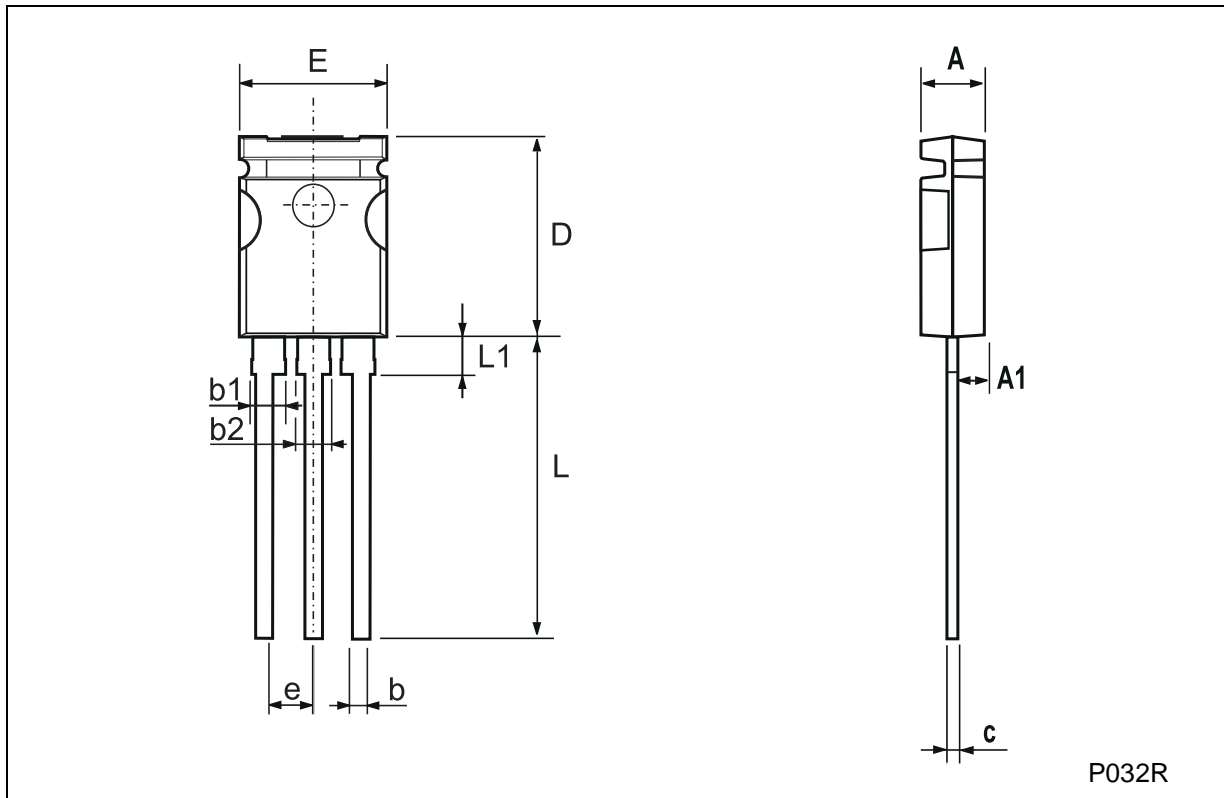
ISOWATT220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.4		0.7	0.015		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	0.385		0.417
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



SOT-82FM MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.85		3.05	1.122		1.200
A1	1.47		1.67	0.578		0.657
b	0.40		0.60	0.157		0.236
b1	1.4		1.6	0.551		0.630
b2	1.3		1.5	0.511		0.590
c	0.45		0.6	0.177		0.236
D	10.5		10.9	4.133		4.291
e	2.2		2.8	0.866		1.102
E	7.45		7.75	2.933		3.051
L	15.5		15.9	6.102		6.260
L1	1.95		2.35	0.767		0.925



P032R

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